KKICU I		
EVALUATION TIME (FOR N BYTES OF INPUT) [ORDER OF]	MEMORY ACCESS CYCLES	R * N CPU CACHE+BRANCH CYCLES
STORAGE BOUND ON # OF STATES (FOR R CHARACTER REGULAR EXPRESSION)	2R (NEEDS VERY LARGE MEMORY)	
PROPERTIES OF DFA AND NFA TECHNIQUES USED ON CONVENTIONAL MICROPROCESSORS	DETERMINISTIC FINITE STATE AUTOMATA OR DFA RUNNING ON A GP CPU	NON-DETERMINISTIC FINITE STATE AUTOMATA NFA RUNNING ON A GP CPU

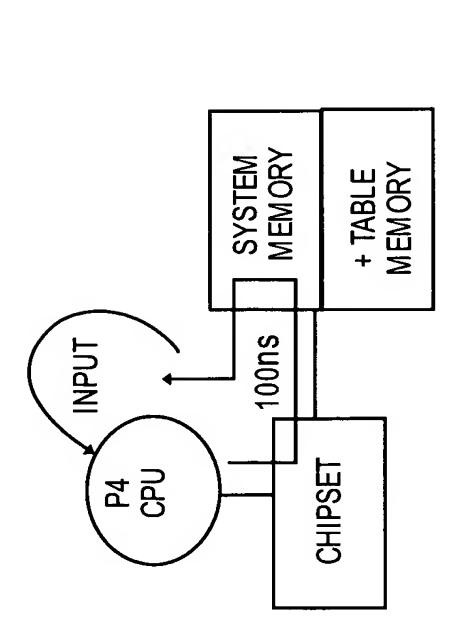
FIG. 1A (PRIOR ART)

TABLE MEMORY

OFFLOAD PROCESSOR

30ns





COPROCESSOR CLOSER TO TABLE IN SRAM SYSTEM MEMORY CHIPSET 99 UG INPUT

PERFORMANCE ON EVALUATING REGULAR EXPRESSIONS ON EVERY BYTE OF INPUT STREAM

1000s OF RES @ 100 Mbps

GIGABYTES OF MEMORY

100s OF RES @ 280 Mbps

100s OF MBs OF SRAM

FIG. 1B (PRIOR ART)